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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9 and 11* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Due to newly found reference, the previously indicated allowability of claims 1-4 and 6-9 has been withdrawn. Consequently, the Final Rejection has also been withdrawn. Examiner regrets the inconvenience this might cause the Applicant.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1,2, 6, and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sokawa** et al. U.S. Pat. No. 6,353,460 in view of **Hwang**, U.S. Patent No. 5,896,177.

Considering claim **1,** Sokawa et al discloses the following claimed subject matter, note;

d) a **format converter** for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the

format converter into a predetermined display format output signal, **is met by the format conversion section 1100, fig.1;**

e) a **controller** for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of the input digital signal, **is met by the CPU 1020, fig. 1;**

Except for;

a) a first phase locked loop;

b) a second phase locked loop;

c) a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal;

Regarding a) and b), Sokawa et al. disclose one PLL circuit. "A clock circuit (not shown) composed of a PLL circuit, for example, for supplying necessary clocks to the respective components of the image processor is also included." (col. 18, lines 32-35) [emphasis added by Examiner]

Hwang discloses a device controlling an aspect ratio in TV-Monitor integrated wide screen receiver. Specifically, Hwang teaches a phase-locked loop system (Fig.4) wherein a PLL 70, a PLL 80, a multiplier 64, a switch 66 are illustrated. A horizontal sync signal is inputted to the multiplier 64 and the output of the multiplier (2) and the horizontal sync (1) are then input to the switch 66. The output of the switch 66 is inputted to the PLL 70. When the switch 66 selectively outputs a signal to the PLL

circuit 70 according to the control signal, PLL 70 generates at least two different clock frequency signals as a result. (see col. 4, line 23+)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Sokawa et al. by providing the PLL system of Hwang as proposed above, in order to save space and cost of the system by making the system compact by using only one PLL circuit instead of two PLL circuits as claimed.

Regarding c), the combination of Sokawa et al. and Hwang as modified above in parts (a) and (b) does not disclose a switching means. However, the Examiner takes Official Notice in that it is notoriously well known in the art to utilize a selector or a switching means to select one signal out of a plurality of signals that needs to be processed further, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system as proposed above, by providing a switch to select one of the clock signals output from the PLL circuit 70.

Considering claim **2**, the apparatus of claim 1, wherein the first phase locked loop generates a clock frequency of 74.25 MHz, and wherein the second phase locked loop generates a clock frequency of 74.175 MHz.

Regarding claim 2, the combination of Sokawa and Hwang as modified above does not specifically disclose generating a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1 and 2, respectively. However, it would have been an obvious matter of design choice to generate a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1

and 2, or a variation thereof, since Applicant has not disclosed that using a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1 and 2 solves any stated problem or is for any particular purpose and it appears that similar clock frequencies, say, 74.20 MHz or 74.26 MHz, etc. would perform equally well.

Considering claim **6**, Sokawa et al. disclose the following claimed subject matter, note; a) the claimed video decoder for decoding a video component of a received digital signal into a first input digital signal, **is met by digital decoder 1017, fig.1;**

b) the claimed analog to digital converter for converting a received analog video signal into a second input digital signal, is implied here because the format conversion section is a digital processing device, not an analog processing device.

c) the claimed a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal into a predetermined display format output signal, **is met by the format conversion section 1100, fig.1;**

d) the claimed controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected, **is met by the CPU 1020, fig. 1**;

Except for;

e) the clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal, said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter;

f) wherein said clock frequency providing means comprises: a first phase locked loop for generating a first clock frequency; a second phase locked loop for generating a second clock frequency; anda switching portion that receives said timing control signal from said controller and said switching portion outputting one of said first and second clock frequencies corresponding to the received timing control signal as said clock frequency.

Regarding e) and f), Sokawa et al. do not specifically disclose two PLL circuits. However, Sokawa et al teach, "A clock circuit (not shown) composed of a PLL circuit, for example, for supplying necessary clocks to the respective components of the image processor is also included." (col. 18, lines 32-35) [emphasis added by Examiner]

Hwang discloses a device controlling an aspect ratio in TV-Monitor integrated wide screen receiver. Specifically, Hwang teaches a phase-locked loop system (Fig.4) wherein a PLL 70, a PLL 80, a multiplier 64, a switch 66 are illustrated. A horizontal sync signal is inputted to the multiplier 64 and the output of the multiplier (2) and the horizontal sync (1) are then input to the switch 66. The output of the switch 66 is

inputted to the PLL 70. When the switch 66 selectively outputs a signal to the PLL circuit 70 according to the control signal, PLL 70 generates at least two different clock frequency signals as a result. (see col. 4, line 23+)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Sokawa et al. by providing the PLL system of Hwang as proposed above, in order to save space and cost of the system by making the system compact by using only one PLL circuit instead of two PLL circuits as claimed.

Considering claim **11**, (previously presented): A method of adapting clock frequency in digital signal receiver to correspond with a frame rate of an input broadcast signal, said method comprising: receiving said input broadcast signal into said digital signal receiver; detecting a frame rate of the input broadcast signal received; selecting a clock frequency that corresponds to the frame rate which is detected; and outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to convert the input broadcast signal into a predetermined display format output signal; wherein the step of selecting the clock frequency comprises, outputting a control signal from a controller, said control signal depending upon the frame rate which is detected; receiving said control signal into a selector, said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, and selecting one predetermined clock

frequency of one of said plurality of phase locked loops based upon the control signal received by the selector.

Regarding claim **11**, see rejection of claim 6.

4. Claims **7-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sokawa** et al. U.S. Pat. No. 6,353,460 in view of **Hwang**, U.S. Patent No. 5,896,177 as applied to claims 6 and 11 above, and further in view of Bestler et al., U.S. Pat. No. 5,638,112.

Considering claim **7**, the digital signal receiver according to claim 6, further comprising an onscreen graphics mixer for mixing desired graphics with said predetermined display format output signal to output a mixed graphics video signal, wherein said on-screen graphics mixer operates responsive to the clock frequency provided by said clock frequency providing means.

Regarding claim 7, the television receiver system of the Sokawa et al reference discloses an image processor 1040 within the format converter 1100. Sokawa and Hwang, as modified above, do not specifically disclose an OSD mixer. However, as well known in the art television receivers such as the Sokawa reference would utilize OSDs and mixers that would be used to mix or blend image signals with graphics or OSD signals. In that regard, Bestler et al. disclose a hybrid analog/digital STB wherein an MPEG decoded image signal is mixed with OSD generated signal in the digital mixer 60 (Figure). Therefore, it would have been obvious to the skilled in the art at the time

the invention was made to modify the combined system of Sokawa et al. and Hwang by providing the mixer of Bestler et al. so that the system would be made more versatile and useful.

Considering claim **8**, the digital signal receiver according to claim 7, further comprising a video signal processor for processing the mixed graphics video signal output from said on-screen graphics mixer;

Regarding claim 8, the system as modified above does not specifically disclose an video signal processing (VSP) means. However, the Examiner takes Official Notice in that it is notoriously well known in the art to utilize a video signal processor to process the video signal, and therefore, it would have been obvious to the skilled in the art to modify the system, by providing a VSP, because otherwise the video signals might not be displayed correctly.

Considering claim **9**, the digital signal receiver according to claim 7, further comprising audio signal processing means for processing audio signals received in said digital signal receiver.

Regarding claim 9, again, the system as modified above does not specifically disclose an audio signal processing means. However, the Examiner takes Official Notice in that it is notoriously well known in the art to utilize an audio signal processor to process the audio signal, and therefore, it would have been obvious to the skilled in the

art to modify the system, by providing an audio signal processor, so that the audio signal is reproduced properly at the speakers of the system or any other output.

Allowable Subject Matter

5. Claims **3 and 4** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose, an apparatus selectively converting a clock frequency in a digital signal receiver, comprising: *wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 Hz and 23.97 Hz,* ***wherein if the frame rate of the input digital signal is one of 60 Hz, 30Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop****, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz,* ***the controller controls the switching portion to select the clock frequency from the second phase locked loop***, as in claim **3**;

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kohiyama et al. discloses a digital PLL circuit for MPEG stream and MPEG decoder having the digital PLL circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
June 11, 2004

MICHAEL H. LEE
PRIMARY EXAMINER